RESEARCH ARTICLE OPEN ACCESS

A Revive on 32×32 Bit Multiprecision Dynamic Voltage Scaling Multiplier with Operands Scheduler

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ABSTRACT
In this paper, we present a Multiprecision (MP) reconfigurable multiplier that incorporates variable precision, parallel processing (PP), razor-based dynamic voltage scaling (DVS), and dedicated MP operands scheduling to provide optimum performance for a variety of operating conditions. All of the building blocks of the proposed reconfigurable multiplier can either work as independent smaller-precision multipliers or work in parallel to perform higher-precision multiplications. Given the user's requirements (e.g., throughput), a dynamic voltage/ frequency scaling management unit configures the multiplier to operate at the proper precision and frequency. Adapting to the run-time workload of the targeted application, razor flip-flops together with a dithering voltage unit then configure the multiplier to achieve the lowest power consumption. The single-switch dithering voltage unit and razor flip-flops help to reduce the voltage safety margins and overhead typically associated to DVS to the lowest level. The large silicon area and power overhead typically associated to reconfigurability features are removed. Finally, the proposed novel MP multiplier can further benefit from an operands scheduler that rearranges the input data, hence to determine the optimum voltage and frequency operating conditions for minimum power consumption.
This low-power MP multiplier is fabricated in AMIS 0.35-μm technology. Experimental results show that the proposed MP design features a 28.2% and 15.8% reduction in circuit area and power consumption compared with conventional fixed-width multiplier. When combining this MP design with error-tolerant razor-based DVS, PP, and the proposed novel operands scheduler, 77.7%–86.3% total power reduction is achieved with a total silicon area overhead as low as 11.1%. This paper successfully demonstrates that a MP architecture can allow more aggressive frequency/supply voltage scaling for improved power efficiency

I. Introduction

Consumers demand for increasingly portable yet high performance multimedia and communication products imposes stringent constraints on the power consumption of individual internal components of these, multipliers perform one of the most frequently encountered arithmetic operations in digital signal processors (DSPs). For embedded applications, it has become essential to design more power-aware multipliers. Given their fairly complex structure and interconnections, multipliers can exhibit a large number of unbalanced paths, resulting in substantial glitch generation and propagation. This spurious switching activity can be mitigated by balancing internal paths through a combination of architectural and transistor-level optimization techniques.

In addition to equalizing internal path delays, dynamic power reduction can also be achieved by monitoring the effective dynamic range of the input operands so as to disable unused sections of the multiplier and/or truncate the output product at the cost of reduced precision . This is possible because, in most sensor applications, the actual inputs do not always occupy the entire magnitude of its word-length. For example, in artificial neural network applications, the weight precision used during the learning phase is approximately twice that of the retrieval phase . In contrast, most of today's full-custom DSPs and application-specific integrated circuits (ASICs) are designed for a fixed maximum word-length so as to accommodate the worst case scenario. Therefore, an 8-bit multiplication computed on a 32-bit Booth multiplier would result in unnecessary switching activity and power loss. In Most applications are based on 8–16-b operands, the proposed multiplier is designed to not only perform single 16-b but also performs single 8-b, or twin parallel 8-b multiplication operations. in some applications,16 and 32 bit operands are send to smaller multiplication circuit with parallel operation reduce power consumption and also reduces area over head.

Due to the complex structure and interconnections, multipliers have large amount of unbalanced path which causes unwanted signal generation and propagation. This can be avoided by proper internal balancing through architectural and transistor level optimization. in most cases of multipliers, maximum word length is provided. Hence small multiplications are done in large

multipliers, this causes unwanted switching activity and also power consumption. So word length optimization is the best method in which 8-bit multiplier is reused for 16-bit and 32-bit multiplication . Here it is possible to incorporate the pipelining for increasing the speed of the multiplier.

Objective: The objective of this project is to provide optimum performance for the variety of operating conditions. A dynamic voltage scaling (DVS) management unit configures the multiplier to operate at the proper precision and frequency. The novel MP multiplier that rearranges the input data, hence to determine the optimum voltage and frequency operating conditions for minimum power consumption.

II. LITERATURE SURVEY

Several works investigated this word-length optimization. proposed an ensemble of multipliers of different precisions, with each optimized to cater for a particular scenario. Each pair of incoming operands is routed to the smallest multiplier that can compute the result to take advantage of the lower energy consumption of the smaller circuit. This ensemble of point systems is reported to consume the least power but this came at the cost of increased chip area given the used ensemble structure. To address this issue proposed to share and reuse some functional modules within the ensemble. In an 8-bit multiplier is reused for the16-bit multiplication, adding scalability without large area penalty. Reference extended this method by implementing pipelining to further improve the multiplier's performance. A more flexible approach is proposed in , with several multiplier elements grouped together to provide higher precisions and reconfigurability. Reference analyzed the over head associated to such reconfigurable multipliers. This analysis showed that around 10%–20% of extra chip area is needed for 8–16 bits multipliers.

S. Das, C. Tokunaga, S. Pant, W.-H. Ma, S. Kalaiselvan, K. Lai, D. M. Bull, and D. T. Blaauw, "RazorII: In situ error detection and correction for PVT and SER tolerance," *IEEE J. Solid-State Circuits*,vol. 44, no. 1, pp. 32–48, Jan. 2009. Power gating techniques are rapidly gaining popularity assisting the management of leakage power consumption for deep submicrometer microprocessors' functional units. A design (RazorII) which implements a flip-flop with *in situ* detection and architectural correction of variation-induced delay errors. Error detection is based on flagging spurious transitions in the state-holding latch node. The RazorII flip-flop naturally detects logic and register SER**.**

R. Kuang and J.-P. Wang, "Design of power-efficient configurable booth multiplier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 3, pp. 568–580, Mar. 2010. A power-efficient 16times16 configurable Booth multiplier (CBM) that supports single 16-b, single 8-b, or twin parallel 8-b multiplication operations is proposed. To efficiently reduce power consumption, a novel dynamic-range detector is developed to dynamically detect the effective dynamic ranges of two input operands. The detection result is used to not only pick the operand with smaller dynamic range for Booth encoding to increase the probability of partial products becoming zero but also deactivate the redundant switching activities in ineffective ranges as much as possible.

Youssef, M. Anis, and M. Elmasry, "A comparative study between static and dynamic sleep signal generation techniques for leakage tolerant designs," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*,vol. 16, no. 9, pp. 1114–1126, Sep. 2008. A comparative study between the static and dynamic approaches regarding the power-performance tradeoff will be presented. It will be shown that the dynamic sleep signal generator is capable of tracking the operation of the functional units while achieving accuracies up to 90% compared to an average of 40%–60% for the static sleep signal generator (SSSG). Additionally it saves up to 80% more leakage versus the SSSG.[3]

R. Min, M. Bhardwaj, S.-H. Cho, N. Ickes, E. Shih, A. Sinha, A. Wang,and A.Chandrakasan, "Energy-centric enabling technologies for wireless sensor networks," *IEEE Wirel. Commun.*, vol. 9, no. 4, pp. 28–39, Aug. 2002. Advocate two particular enablers for energy conservation: the ability to trade off performance for energy savings within the node, and collaborative processing among nodes to reduce the overall energy dissipated in the network. New levels of energy efficiency — attained through global system-level perspectives on node and network energy consumption — will enable a future where networks of hundreds, thousands, and eventually many millions of collaborating nodes are as commonplace as today's cellular phone.

F. Carbognani, F. Buergin, N. Felber, H. Kaeslin, and W. Fichtner, "Transmission gates combined with level-restoring CMOS gates reduce glitches in low-power low-frequency multipliers," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 16, no. 7, pp. 830–836, Jul. 2008.

Various 16-bit multiplier architectures are compared in terms of dissipated energy, propagation delay, energy-delay product (EDP), and area occupation, in view of low-power low-voltage signal processing for low-frequency applications. A novel practical approach has been set up to investigate and graphically represent the mechanisms of glitch generation and propagation. It is found that spurious activity is a major cause of energy dissipation in multipliers. Measurements point out that, because of its shorter full-adder chains, the Wallace multiplier

dissipates less energy than other traditional array multipliers (8.2 W/MHz versus 9.6 W/MHz for 0.18-m CMOS technology at 0.75 V). The benefits of transistor sizing are also evaluated (Wallace including minimum-size transistors dissipates 6.2 W/MHz). By combining transmission gates with static CMOS in a Wallace architecture, a new approach is proposed to improve the energy-efficiency further (4.7 W/MHz), beyond recently published low-power architectures. The innovation consists in suppressing glitches via resistance–capacitance low-pass filtering, while preserving unaltered driving capabilities. The reduced number of Vdd-to-ground paths also contributes to a significant decrease of static consumption.

III. SUMMARY

Input oriented voltage scaling multiplier can overcome the drawback of conventational system where power and circuit area is wasted by disabling unused section of multiplier.
By this there is reduction in path delays and unwanted switching.

Problem Definition:

Configurable booth multipleir detect the effective dynamic ranges of two input operands in ineffective ranges.In the previous experimental results show that the proposed MP design features a 28.2% and 15.8% reduction in circuit area and power consumption compared with conventional fixed-width multiplier. This method have some limitations.

IV. METHODOLOGY PROPOSED SYSTEM

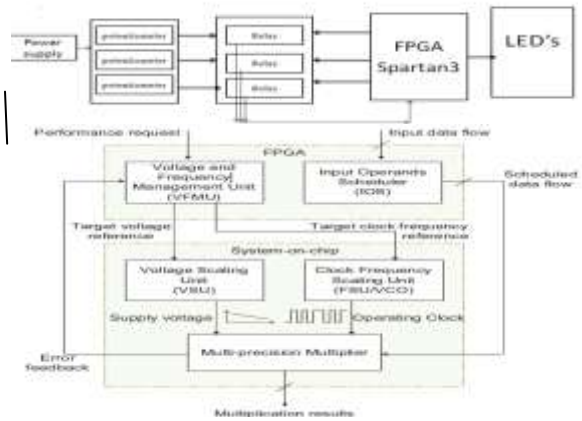


Fig. Overall multiplier system architecture

1) IOS (Input operand scheduler):

The input operands scheduler which rearranges the input data and hence reduce the supply voltage transition, thus power consumption will be reduced. It consists of range detector, buffer (RAM), and a voltage and frequency analyzer. These help to rearrange the input and detect the precision and send to MP multiplier. Here proposed an IOS that will perform the following tasks:

1) Reorder the input data stream so that same-precision operands are grouped together into a buffer and

2) takes the minimum supply and frequency from the LUT.

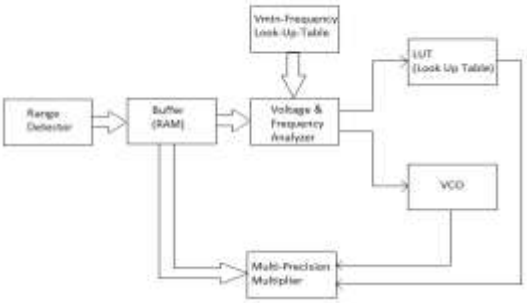


Fig. Input Operands Scheduler

2) Frequency Scaling Unit

Frequency scaling unit of proposed MP multiplier is used for frequency tuning to meet the system throughput requirements. The frequency scaling unit is one which equipped with VCO is used to select frequency for each combination of multiplication. Depending on the control signal, it gives frequency that pre-calculated for 8 x 8bit, 16 x 16 bit and 32 x 32 bit for proper multiplication to reduce delay. Depending on the voltage VCO adjust the frequency. For each combination of multiplication, we can select the corresponding suitable frequency.

3) Voltage scaling Unit

The voltage scaling unit (VSU) , its function is to dynamically generate the supply voltage so as to minimize power consumption.

4) Voltage /frequency management unit

The dynamic voltage/frequency management unit (VFMU) that receives the user requirements (e.g. throughput).The VFMU sends control signals to the VSU and FSU to generate the required power supply voltage and clock frequency for the MP multiplier.

MP MULTIPLIER:

Combining multiprecision (MP) with dynamic voltage scaling (DVS) can provide a dramatic run-time workload rather than fixing it to cater for the worst case scenario. When adjusting the voltage, the actual performance of the multiplier running under scaled voltage has to be characterized to guarantee a fail-safe operation. Conventional DVS techniques consist mainly of lookup table (LUT) and on-chip critical path replica approaches. The LUT approach tunes the supply voltage according to a predefined voltage-frequency relationship stored in a LUT,

which is formed considering worst case conditions (process variations, power supply droops, temperature hot-spots, coupling noise, and many more). Therefore, large margins are necessarily added, which in turn significantly decrease the effectiveness of the DVS technique. The critical path replica approach typically involves an on-chip critical path replica to approximate the actual critical path. Therefore, voltage could be scaled to the extent that the replica fails to meet the timing. However, safety margins are still needed to compensate for the intradie delay mismatch and address fast-changing transient effects.

1) A novel MP multiplier architecture featuring, respectively, 28.2% and 15.8% reduction in silicon area and power consumption compared with its conventional 32 × 32 bit fixed-width multiplier counterpart. All reported multipliers trade silicon area/power consumption for MP . In this paper, silicon area is optimized by applying an operation reduction technique that replaces a multiplier by adders/subtractors.
2) A silicon implementation of this MP multiplier integrating an error-tolerant razor-based dynamic DVS approach. The fabricated chip demonstrates run-time adaptation to the actual workload by operating at the minimum supply voltage level and minimum clock frequency while meeting throughput requirements. Prior works combining MP with DVS have only considered a limited number of offline simulated precision-voltage pairs, with unnecessary large safety margins added to cater for critical paths .
3) A novel dedicated operand scheduler that rearranges operations on input operands so as to reduce the number of transitions of the supply voltage and, in turn, minimize the overall power consumption of the multiplier. Unlike reported scheduling works, the function of the proposed scheduler is not task schedulingrather input operands scheduling for the proposed MP multiplier.

The proposed MP multiplier system comprises five different modules that are as follows:

1) The MP multiplier;

2) The input operands scheduler (IOS) whose function is to reorder the input data stream into a buffer, hence to reduce the required power supply voltage transitions;

3) The frequency scaling unit implemented using a voltage controlled oscillator (VCO). Its function is to generate the required operating frequency of the multiplier;

4) The voltage scaling unit (VSU) implemented using a voltage dithering technique to limit silicon area overhead. Its function is to dynamically generate the supply voltage so as to minimize power consumption;

5)The dynamic voltage/frequency management unit (VFMU) that receives the user requirements (e.g., throughput).

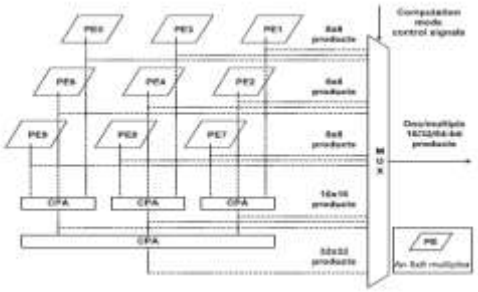


Fig.3.3 Possblie configuration modes of proposed MP multiplier.

REQUIREMENTS:

- Hardware Requirement
- Potentiometer 10K
- Relay (SPDT)
- FPGA Spartan -3
- LED'S
- Software Requirement
- Xilinx
- Hardware description Language
- Verilog.

FPGA SPARTAN -3

Board features

- FPGA: Spartan XC3S50A in TQG144 package
- Flash memory: 16 Mb SPI flash memory (M25P16)
- USB 2.0 interface for On-board flash programming
- FPGA configuration via JTAG and USB
- 8 LEDs, Six Push Buttons and 8 way DIP switch for user defined purposes
- One VGA Connector
- One Micro SD Card Adapter
- Three Seven Segment Displays
- 39 IOs for user defined purposes
- On-board voltage regulators for single power rail operation

V. POTENTIOMETER

Three **10k** potentiometer is used**.**

- 1st potentiometer is used to set 3.3V
- 2nd potentiometer is used to set 2.8V
- 3rd potentiometer is used to set 1.8V

RELAY (SPDT)

One Stereo Jack relay is an electrically operated switch. Current flowing through the coil of the relay creates a magnetic field which attracts a lever and changes the switch contacts. The coil current can be on or off so relays have two switch positions and they are double throw (changeover) switches.

The relay's switch connections are usually labelled COM, NC and NO:

- **COM** = Common, always connect to this, it is the moving part of the switch.
- **NC** = Normally Closed, COM is connected to this when the relay coil is **off**.
- **NO** = Normally Open, COM is connected to this when the relay coil is **on**.
- Connect to COM and NO if you want the switched circuit to be **on when the relay coil is on**.
- Connect to COM and NC if you want the switched circuit to be **on when the relay coil is off**.

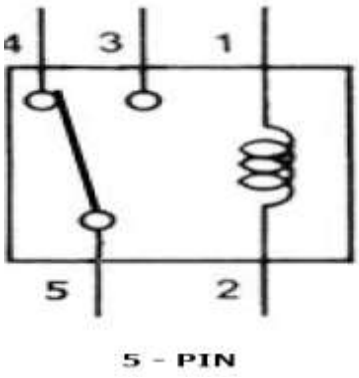


Fig. Relay

SOFTWARE

Xilling 14.5 is used . These are the following steps which are important to create new project.

VI. HARDWARE DISCRIPTION LANGAUGE

- They are Hardware description languages.
- They are each a notation to describe the behavioral and structural aspects of an electronic digital circuit.

VERILOG

- Verilog only has one building block
- Module: modules connect through their port similarly as in VHDL
- Usually there is only one module per file.
- A top level invokes instances of other modules.
- Modules can be specified behaviorally or structurally.
- Behavioral specification defines behavior of digital system
- Structural specification defines hierarchical interconnection of sub modules .

ADDERS

Variable latency adders have been recently proposed in literature. A variable latency adder employs speculation: the exact arithmetic function is replaced with an approximated one that is faster and gives the correct result most of the time, but not always.

The paper describes the stages in which variable latency speculative prefix adders can be subdivided and presents a novel error detection network that reduces error probability compared to previous approaches. Several variable latency speculative adders, for various operand lengths, using both Han-Carlson and Kogge-Stone topology. Obtained results show that proposed variable latency Han-Carlson adder outperforms both previously proposed speculative Kogge-Stone architectures and non-speculative adders, when high-speed is required.

- **Basic Adder Unit**

A combinational circuit that adds two bits is called a half adder. A full adder is one that adds three bits, the third produced from a previous addition operation.

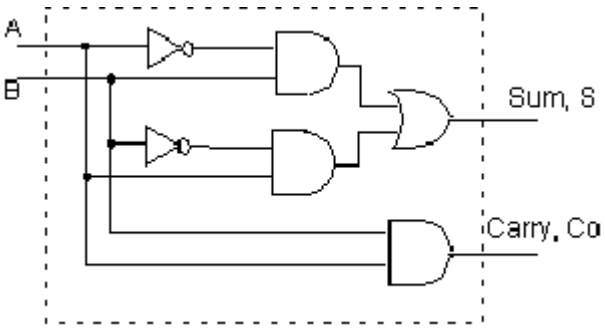
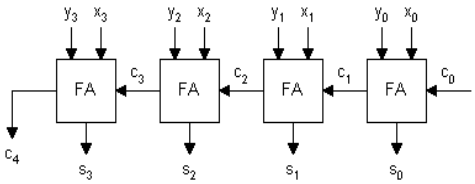


Fig.Half Adder and Full Adder Boolean equation

Sum=A xor B xor Cin;
Carry=(A and B)or(A and Cin)or (B and Cin);
Its mean one full adder consist 7 gates is below 2 xor,3 and ,2 or gates.

- **Ripple Carry Adder**

The ripple carry adder is constructed by cascading full adder blocks in series. The carryout of one stage is fed directly to the carry-in of the next stage. For an n-bit parallel adder, it requires n full adders.



3.6 Ripple Carry Adder

If we taken the 16 bit Ripple carry adder mean its consist of 16 full adder. One full adder consist of 7 gates mean 16 bit Ripple carry adder consist of 16*7=112 gates.

- **Carry Look-Ahead Adder**

Calculates the carry signals in advance, based on the input signals

Boolean Equations

$P_i = A_i \oplus B_i$ Carry propagate

$G_i = A_iB_i$ Carry generate

$S_i = P_i \oplus C_i$ Sum

$C_{i+1} = G_i + P_iC$ Carry out

Signals P and G only depend on the input bits. If we taken 16 bit adder means it required 135 gates.

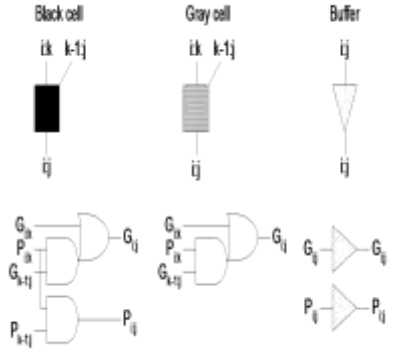


Fig. Notations of Cell

- **Kogge-Stone Adder**

One black cell consist of 3 gates is 2 and , one or gate. Kogge- stone adder consist of 33 black cell 35*3=105 gates is required .

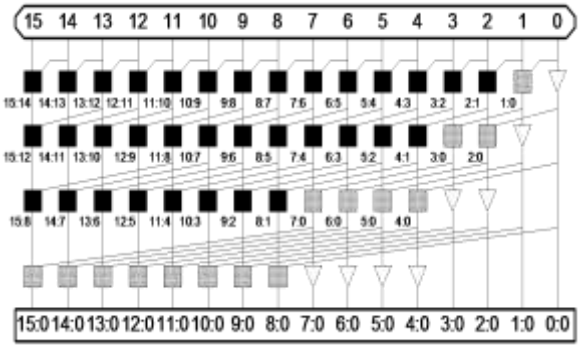


Fig. Kogge stone Adder

Comparison:

Adder	Required gates
Ripple carry adder	112
Carry look ahead adder	135
Kogge stone adder	105

Table.Comparisons of Adders

VII. REVERSIBLE LOGIC MULTIPLICATION

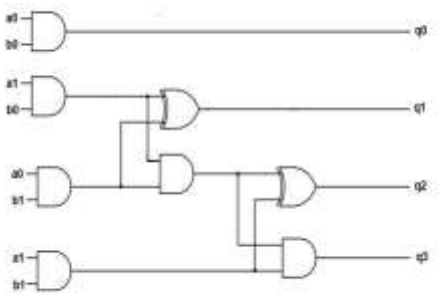


Fig.2x2 multiplier using conventional logic

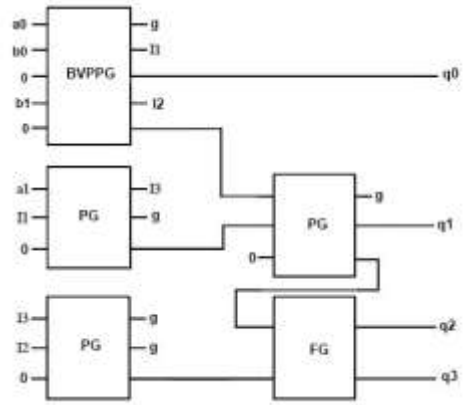


Fig. Reversible implementation of 2x2 Vedic multiplier

1) **Feynman Gate**: It is 2x2 gate. If the first input i.e. A is given as 1 the second output will be the complement of the second input i.e. B. so, this gate is also known as Controlled Not Gate. It can also be used to copy inputs. Quantum cost of this gate is one.
2) **Peres Gate**: It is a 3x3 gate. It can be used as a half adder with third input i.e. c as 0.It also serves the purpose of fan out. Quantum cost of this gate is four.
3) **HNG Gate**: It is a 4x4 gate. A single HNG gate can serve as a one bit full adder. Quantum cost of this gate is six.
4) **BVPPG gate**: In this 5x5 reversible gate is proposed. It is basically for multiplication and can generate two partial products at a time. Quantum cost of this gate is ten.

The existing method of multiplier in this method using the six AND gate and two XOR gates for 2x2 multiplier but if we using the reversible gate as shown in fig then we required the only five gates.

Then if we use the less gates then we required less power ,less Area and also increase the speed.

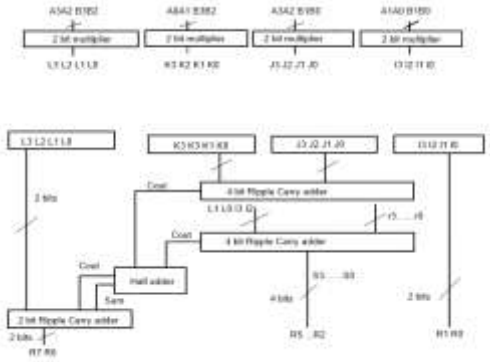


Fig.4x4 Vedic multiplier.

ADVANTAGES:
1) Reduse power.
2) Increase speed.
3) Decrease delay.
4) Decrease Area .
5) Increase performance.

Experimental Simulation System Flow

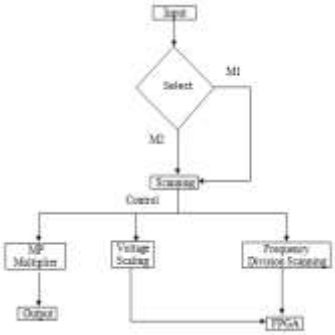


Fig. System Flow

Frequency Division Scanning

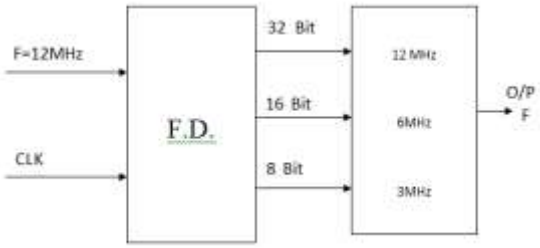


Fig. Frequency Division scanning

In frequency division scanning shown in fig. we use 12MHz frequency. Clk and input frequency is given to the frequency division. Frequency division block divide the frequency in three frequencies that are 12MHz, 6MHz and 3MHz. The 12MHz, 6MHz and 3MHz frequency is use for 32 Bit, 16 Bit and 8 Bit respectively as per the input.

Input Scanning

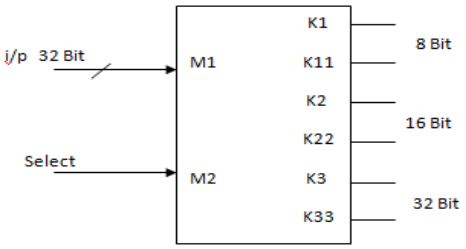


Fig. Input Scanning

In input scanning, we use 32 bit input and select. The 32 bit input and selctore is used to reduce the number of gates. The M1 and M2 are the two input multiplier. If the select is 0, then it selects M1 and if select is at 1, then device selects M2 multiplicant. In input scanning there are six output lines K1,K11,K2,K22,K3 and K33. The K1 and K11 are use for 8 bit operation, K2and K22 are used for 16 bit operation and K3 and K33 for 32 bit operation. If the multiplicant M1 is of 8 bit and another multiplicant M2 is of 16 bit then the input scanning selects higher number of bit i.e. 16 bit at output line and it is also same for 32 bit .Each bit has control select. For 8 bit we use control 1, for 16 bit we use control 2 and for 32 bit we use control 3 lines.

Simulation of Frequency Division Scanning

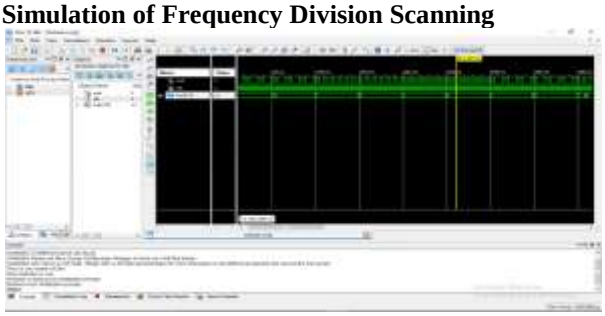


Fig. Simulation of FDS

Remark: The result of frequency division scanning simulation is in table,

Input Control Signal	Output
01	3MHz
10	6MHz
11	12MHz

Table .Input Output of FDS

Simulation of Input Scanning

Fig. Simulation of Input Scanning

Remark: the result of input scanning simulation is in table,

Remaining Work to Implement

1. MP Multiplier

For 8×8 bit, 16×16 bit and for 32×32 bit multiplication the MP multiplier we will use. For the multiplication we use reversible gates instead of other multiplication methods i.e. mux. For the adding the partial product term in multiplication we use kogge stone adder instead of carry loop adder.

2. Voltage Scanning Unit

In voltage scanning unit, it will select the required voltage. For 8 bit,16 bit and 32 bit of multiplication we will use 1.2, 2.2 and 3.3v respectively.

3. Top Module

In top module we combine all the models. In this MP multiplier, voltage scanning, and frequency division scanning unit will combine in FPGA.

VIII. Summary and Discussion

Conclusion

In this peoject, the input scanning is for to scan the input, which is of 8 bit, 16 bit or 32 bit. From this scanning the control signal is grnerated. Then control signal is send to the MP multiplier, voltage scanning, frequency division scanning and to the FPGA. The frequency division scanning is divede the frequency of 12MHz into 3MHz , 6MHz and 12MHz. The 3MHz of frequency is used for 8 bit input, 6MHz of frequency is for 16 bit of input and 12MHz of frequency is for 32 bit input. The input scanning is also selects the multiplication bit that is divided into 3 output bits, 8bit ,16 bit and 32 bit. It will give priority to the highest number of bit.

Advantages:

- Reduction in silicon area and power consumption compared with its 32 × 32 bit conventional fixed-width multiplier counterpart.
- run-time adaptation to the actual workload by operating at the minimum supply voltage level and minimum clock frequency.
- The key advantage of Razor over existing voltage scaling technologies is the use of in-situ timing error detection and correction, permitting increased energy reduction because voltage margins are completely eliminated.

Applications:

- In DSP

This is used in digital signal processors for arithmetic operation. In the DSP, there are many multiplication operation are done at the background. By using this MP multiplier we can increase the speed of DSPs.

- For embedded application

It is has become essential to design more power aware multiplier. In embedded applications also there are many multiplication operations are run, so this application will decreases the power required to rum the circuit.

- This can be improve power efficiency by frequency, voltage scaling. And also it improves the performance of the circuit.

Sr. No.	Input		Output						
	M1	M2	Control	8 Bit		16 Bit		32 Bit	
				K1	K11	K2	K22	K3	K33
1.	234	21453	Control 2	X	X	234	21453	X	X
2.	2456374	99	Control 3	X	X	X	X	2456374	99
3.	23346	15000	Control 2	X	X	23346	15000	X	X

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